Curriculum Vitae

Doh Yon Kim

+82-10-4849-7530
andrewdoyon@skku.edu
Department of Electronic and Electrical Engineering
Sungkyunkwan University (SKKU), Republic of Korea

EDUCATION

Sungkyunkwan University — Suwon, Republic of Korea
B.S. in Electronic and Electrical Engineering — Expected Aug. 2026
Double Major in Advanced Semiconductor Engineering

Gyeonggibuk Science High School — Uijeongbu, Republic of Korea
Specialized High School for Academically Gifted Students — Mar. 2017 – Feb. 2020

RESEARCH INTERESTS

Computer Architecture, Neural Processing Units, Hardware-Software Co-Design, FPGA-based Acceleration.

PROFESSIONAL EXPERIENCE

Rebellions (AI Chip Startup) — Seongnam, Republic of Korea
Hardware Engineer Intern – Tape-out Participation — Jun. 2025 – Present

- **NPU Memory Subsystem & NoC Analysis** (Oct. 2025 – Present)
  - Developing an automated SRAM compiler to generate parameterized memory wrappers with built-in clock domain crossing logic and error protection, improving reliability for datacenter-scale NPUs.
  - Analyzing on-chip mesh router topology to identify deadlock points; collaborating on architectural solutions for deadlock-free packet routing.
- **Hash Algorithm Accelerator** (Jun. 2025 – Oct. 2025)
  - Led logic design in a three-person team to develop a SHA-512 accelerator using HLS and OpenCL, spanning from microarchitecture exploration to FPGA deployment.
  - Achieved 2.4 GH/s throughput and improved performance-per-watt by 14.2% over the RTX 4080 via loop unrolling and dataflow pipelining.
  - Architected a distributed system leveraging dual-FPGA clustering to scale throughput for high-volume client workloads.

PUBLICATIONS & PREPRINTS

Doh Yon Kim et al., "UAV-NAS: Novel UAV Identification using Neural Architecture Search on FPGAs" *IEEE Transactions on Industrial Informatics* (Under Review).

- Designed the algorithms and HLS optimizations for a neural architecture search framework.
- Achieved 88.6% energy reduction compared to CPU implementations while maintaining real-time throughput.

ACADEMIC PROJECTS

Llama2.c Acceleration on FPGAs — Dec. 2024 – Aug. 2025

- *Finalist, Creative Innovation Research Program.*

- Investigated HLS optimization strategies to accelerate large language models on FPGA platforms, focusing on memory bandwidth bottlenecks.

High-Level Synthesis Library for Deep Learning Dec. 2024 – Jul. 2025

- *Finalist, Co-Deep Learning Project.*
- Developed a modular HLS library to streamline the deployment of deep learning models, bridging the gap between software frameworks and hardware implementation.

TECHNICAL SKILLS

- **Languages:** Verilog, SystemVerilog, C/C++, Python, OpenCL, Tcl.
- **Tools & Frameworks:** Vivado, Vitis HLS, Synopsys VCS, Verdi, PyTorch.
- **Hardware:** Xilinx FPGAs (Alveo U250, Zynq), ASIC Design Flow.

HONORS, AWARDS & SERVICE

Joint Service Achievement Medal Mar. 2024

Awarded by the UNC/CFC/USFK Commander (Four-Star General)

- Recognized for exemplary leadership in developing and executing the U.S. Army's CBRN response plan during joint training exercises.

KATUSA (Korean Augmentation to the U.S. Army) Aug. 2022 – Feb. 2024

Sergeant, CBRN Non-Commissioned Officer in Charge (NCOIC)

- Served as a liaison and interpreter for U.S. Defense agencies (DTRA, DOE) and Republic of Korea military officials throughout the full term of service.